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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,756	11/03/2003	Albert Sun	P900384	4258

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
10/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,756	SUN ET AL.	
	Examiner	Art Unit	
	HETUL PATEL	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 23, 2008 has been entered.

2. Claims 1-17 were previously cancelled; and claims 18-30 were pending. None of the claims are cancelled; amended or newly added with current RCE. Therefore, claims 18-30 are currently pending in this application.

3. Applicant's arguments filed on September 23, 2008 have been considered but they are not deemed to be persuasive.

4. The rejection of claims 18-30 as in the last office is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 18-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Sun et al. (USPN: 6,401,221) hereinafter, Sun.

As per claim 18, Sun teaches a fault-tolerant system (shown in Fig. 1) on an integrated circuit (see claim 37 of Sun), comprising:

- a configurable logic array (i.e. the programmable flash memory; see Col. 4, lines 31-35);
- a boot program (i.e. 102 in Fig. 1) stored in a programmable memory region, which is executed during system initialization (see Col. 4, lines 4-11);
- a mini-boot code (i.e. 107 in Fig. 1) stored in a protected memory region, which is an alternative set of system initialization instructions and executed when there is an error during an in-circuit program process (see Col. 4, lines 20-29), wherein the mini-boot code comprises a configuration load program designed to access a configuration data from a default location (i.e. (i) the mini-boot code fetches the instruction which causes the CPU 112 to restart the ICP process by first *reading/accessing a value from the remote host address register 120;* see Col. 5, lines 36-40. NOTE: the claimed "accessing" limitation can also be equated with (ii) "fetching instructions (which considered as *accessing data*) from a default location of the protected memory; see step 218 in Fig. 2 and Col. 6, lines 11+); and
- a processor (i.e. CPU 112 in Fig. 1) coupled to the programmable memory region, the protected memory region and the configurable logic array, for

executing instructions from the programmable memory region or the protected memory region (see Col. 4, lines 36-51).

As per claim 19, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the processor boots from the mini-boot code instead of the boot program if the system is rebooted during the in-circuit program process (see Col. 4, lines 43-47).

As per claim 20, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the configurable logic array has a programmable configuration defined by configuration data stored in programmable configuration points within the configurable logic array (i.e. defined by the boot programs 102 and utility programs 104 stored in the programmable flash memory; see Col. 4, lines 31-35).

As per claim 21, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the processor takes a boot vector (i.e. the jump boot vector 116 in Fig. 1) which points to the mini-boot code during system initialization when the in-circuit program process is not completed (see Col. 4, lines 43-47).

As per claim 22, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the processor further couples to a remote host address register (i.e. 120 in Fig. 1), which contains a backup copy of a remote host address (see Col. 4, lines 51-54).

As per claim 23, Sun teaches the claimed invention as described above and furthermore, Sun teaches a multiplexer (i.e. 110 in Fig. 1) coupled to the processor to select the boot program or the mini-boot code during system initialization according to

an in-circuit program process status (i.e. based on ICP status 118 in Fig. 1) (see Col. 4, lines 41-43).

As per claim 24, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the mini-boot code causes the processor to restart a configuration load process by reading the remote host address register to determine which remote host to contact in order to reinitiate the configuration load process (see Col. 5, lines 36-40).

As per claim 25, Sun teaches the claimed invention as described above and furthermore, Sun teaches that the default location is one of an on-chip non-volatile memory (i.e. (i) the remote host address register 120 in Fig. 1 OR (ii) the protected memory where 107 is stored; see step 218 in Fig. 2 and Col. 6, lines 11+) and a host (i.e. 136, 138 and 140 shown in Fig. 1) expected to be coupled with the integrated circuit (i.e. the integrated circuit, which is the combination of 112, 100, 118 and 116 according to claim 37 of Sun, is coupled with remote hosts 136, 138 and 140 via internet 134 as shown in Fig. 1).

As per claims 26-30, refer arguments with respect to the rejection of claims 18-19, 21, 24 and 25, respectively. Claims 26-30 are also rejected based on the same rationale as the rejection of claims 18-19, 21, 24 and 25, respectively.

Remarks

6. As to the remark, Applicant asserted that

(a) The claimed "configurable logic array" is known in the electronics field, also, as a programmable logic device (PLD), field programmable gate array (FPGA) or programmable logic array (PLA) (see paragraph [0003] of the specification). A person having skill in the pertinent art recognizes that a "configurable logic array" is dramatically and fundamentally distinct from a (programmable) flash memory (or other volatile/non-volatile memory). The cited Sun prior art not disclosing the claimed "configurable logic array" or the like. Applicants therefore respectfully submit that the claimed invention is not anticipated by the cited prior-art content of Sun.

(b) Applicants respectfully disagree with the asserted equating between the claimed “configuration data” and the “instructions” of Sun. It is well known in the art that “instructions" are more or less directly utilized to cause a processor (e.g., CPU) to perform specific operations. Quite to the contrary, “configuration data" contains and conveys information that is passively operable by a processor (e.g., CPU) or control logic. Applicants respectfully note that it is illogical or even chaotic to replace Sun's “instructions" with the claimed “configuration data." Following such a replacement, to the extent even hypothetically sensical, the Sun system would cease to function as a consequence of the “configuration data" not causing the processor (e.g., CPU) to perform any operation. As the “configuration data" term of

Applicants' claims is quite distinct from the “instructions" term of Sun in one or more of essence and substance, it may be concluded without doubt that the claimed "configuration data" in a configurable logic array cannot be likened or equated to "instructions" in the flash memory of Sun.

(c) The "configuration load program" term in the independent claims, using the same rationale as set forth above, it may be comfortably concluded without hesitation that the disclosure of Sun also does not anticipate the claimed "configuration [data] load program" simply because, for example, the cited prior art of Sun does not disclose any configurable logic array.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), in response to applicant's arguments that the reference fail to show certain features of applicant’s invention, it is noted that the features upon which applicant relies (i.e., the “configurable logic array” is one of a programmable logic device (PLD), field programmable gate array (FPGA) or programmable logic array (PLA)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, since the flash memory is normally either NAND-type or NOR-type flash memory (i.e. made using array(s) of NAND or NOR (logic) gates) and they are programmable (i.e. configurable), the broad interpretation of the term “configurable logic array” equates it to the programmable flash memory (i.e. configurable/programmable array(s) of NAND or NOR

(logic) gates). Examiner would like to suggest Applicant to amend the pending claim(s) in such a way so it's supported by the original disclosure and overcome the above interpretation.

With respect to (b), Examiner would like to point out to Applicant that the currently pending claim(s) does not clearly define what is and what is not included in the claimed configuration data. Furthermore, the mini-boot code instructions can be modified outside the ICP process of normal boot programs in Sun (i.e. instructions are configurable; see Col. 4, lines 20-23). Hence, Examiner respectfully maintains that the claimed "configuration data" is correctly equated with the "instructions" of the Sun prior art; and claims 18-30 are anticipated by Sun.

With respect to (c), Sun does teach the claimed limitation of "the configuration load program mini-boot code comprises a configuration load program designed to access a configuration data from a default location" by disclosing that the mini-boot code fetches the instruction which causes the CPU 112 to restart the ICP process by first *reading/accessing a value from the remote host address register 120;* see Col. 5, lines 36-40.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hetul Patel/
Hetul Patel
Patent Examiner
Art Unit 2186